What is claimed is:

1. A bipolar transistor comprising:

a semiconductor substrate of a first conductivity type;

a collector region of a second conductivity type, which is defined by isolation regions on the semiconductor substrate;

a first base semiconductor layer of the first conductivity type formed of a silicon germanium (SiGe) layer, which extends from the upper surface of the collector region to the upper surface of the isolation regions;

an emitter region of the second conductivity type formed on the first base semiconductor layer to contact the first base semiconductor layer in a region which is defined by emitter insulating layers formed on the first base semiconductor layer;

second base semiconductor layers of the first conductivity type formed of a silicon layer, which is formed on the portions of the first base semiconductor layer except for the portions having the emitter region and the emitter insulating layers;

base ohmic layers formed on the second base semiconductor layers;

an emitter electrode formed on the emitter region; and

base electrodes formed on the second base semiconductor layers at both sides of the emitter electrode.

2. The bipolar transistor of claim 1, wherein the second base semiconductor layers are formed of an epitaxial growing layer.

3. The bipolar transistor of claim 1, wherein the first conductivity type is p-type and the second conductivity type is n-type.

4. The bipolar transistor of claim 1, further comprising first selectively ion implanted collector (SIC) regions of the second conductivity type, which are formed at portions near the surface of the collector region and adjacent to the isolation regions.

5. The bipolar transistor of claim 1, further comprising a second SIC region of the second conductivity type, which is formed in a portion of the collector region under the emitter region.

6. The bipolar transistor of claim 1, wherein the base ohmic layers are formed of metal silicide.

7. The bipolar transistor of claim 6, wherein the base ohmic layers are formed of one of titanium silicide and cobalt silicide.

8. The bipolar transistor of claim 1, further comprising insulating layers formed between the isolation regions and the first base semiconductor layer, under the base electrodes.

9. The bipolar transistor of claim 8, wherein the insulating layers are formed of one of oxide layers and nitride layers.

10. The bipolar transistor of claim 8, further comprising silicon layers formed between the insulating layers and the first base semiconductor layer.

11. A method of manufacturing a bipolar transistor, the method comprising:

forming a semiconductor substrate of a first conductivity type;

forming a collector region of a second conductivity type, which is defined by isolation regions, on the semiconductor substrate;

forming a first base semiconductor layer of the first conductivity type on the isolation regions and the collector region;

forming emitter insulating layers on the first base semiconductor layer and forming an emitter region of the second conductivity type, of which a contact region to the first base semiconductor layer is defined by the emitter insulating layers;

forming second base semiconductor layers of the first conductivity type formed of silicon layers, on the portions of the first base semiconductor except for the emitter region and the emitter insulating layers;

forming base ohmic layers on the second base semiconductor layers; and

forming base electrodes on the base ohmic layers.

12. The method of claim 11, wherein forming the first base semiconductor layer comprises:

forming a mono-crystalline silicon layer contacting the collector region using a selective epitaxial growing method; and

forming a SiGe layer including impurities of the first conductivity type on the mono-crystalline silicon layer.

13. The method of claim 11, wherein the second base semiconductor layers are formed by a selective epitaxial growing method.

14. The method of claim 13, wherein the second base semiconductor layers are formed at a temperature of 500 to 900°C.

15. The method of claim 11, further comprising forming an emitter of the second conductivity type in a portion of the first base semiconductor layer contacting the emitter region, by performing a thermal treatment on the resultant structure having the emitter region.

16. The method of claim 11, further comprising forming first SIC regions of the second conductivity type in portions of the collector region near the surface of the collector region and adjacent to the isolation regions.

17. The method of claim 11, further comprising forming a second SIC region of the second conductivity type in a portion of the collector region under the emitter region.

18. The method of claim 11, further comprising forming insulating layer patterns, which expose the collector region, on the isolation regions before the first base semiconductor layer is formed.

19. The method of claim 18, further comprising forming silicon layer patterns, which expose the collector region, on the insulating layer patterns.

20. The method of claim 11, wherein the base ohmic layers are formed of metal silicide.